SEMICONDUCTOR MEMORY DEVICE

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Abstract

PURPOSE:To reduce a cell area, to make a capacity large and to obtain a sufficient strength by burying an electrode layer constituting a capacitance into an insulating layer by a method wherein the capacitance of a semiconductor memory device is arranged at the upper part of a first source/drain region and an arrangement part of the capacitance is formed to be an uneven face by forming a recessed part.
CONSTITUTION:A semiconductor memory device has a memory cell which is composed of the following: a first source/drain region and a second source/drain region 5a and 5b; a switching transistor 6 having a gate electrode 4; and a capacitance 15. In the semiconductor memory device, an insulating layer 7 is formed on a semiconductor substrate 1 where the transistor 6 has been formed; a recessed part 10 corresponding to the first source/drain region 5a of the transistor 6 is formed in it. The capacitance 15 where a first electrode layer 11, a dielectric layer 13 and a second electrode layer 14 are laminated is formed inside the recessed part 10; a conductive layer 17 to be used as a bit line is formed, via an interlayer insulating layer 16, on the insulating layer 7 where the capacitance 15 has been formed. The electrode layer 11 of the capacitance 15 is brought into electrical contact with the region 5a; a bit line 18 is brought into electrical contact with the region 5a.